Lecture 10

Adders

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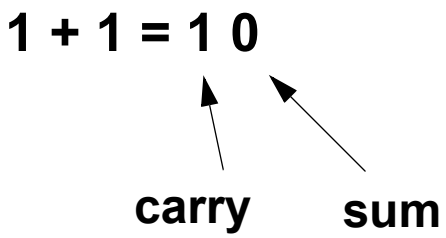
Adders

- **Binary addition**

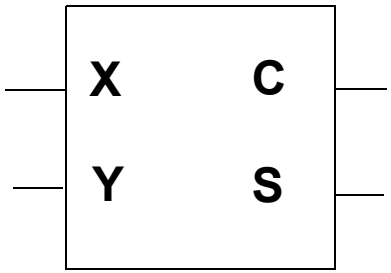
0 + 0 = 0, 0 + 1 = 1, 1 + 0 = 1, 1 + 1 = 10

- **If both numbers are 1, we need two bits to store the result, sum and carry.**



Half Adders

Add two input numbers and generate the sum and carry for the result.



X	Y	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

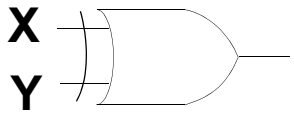
$$C = XY$$

$$S = \overline{X} \cdot Y + X \cdot \overline{Y}$$

XOR Gates

- **XOR generates 1 if the two inputs have different values.**

X	Y	Z
0	0	0
0	1	1
1	0	1
1	1	0

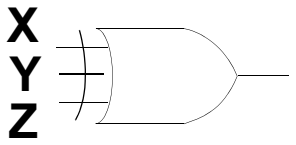


$$Z = X \oplus Y = \overline{X} \cdot Y + X \cdot \overline{Y}$$

N-Input XOR Gates

- **N-input XOR is defined as an odd function, i.e. generates 1 if odd number of inputs are 1.**

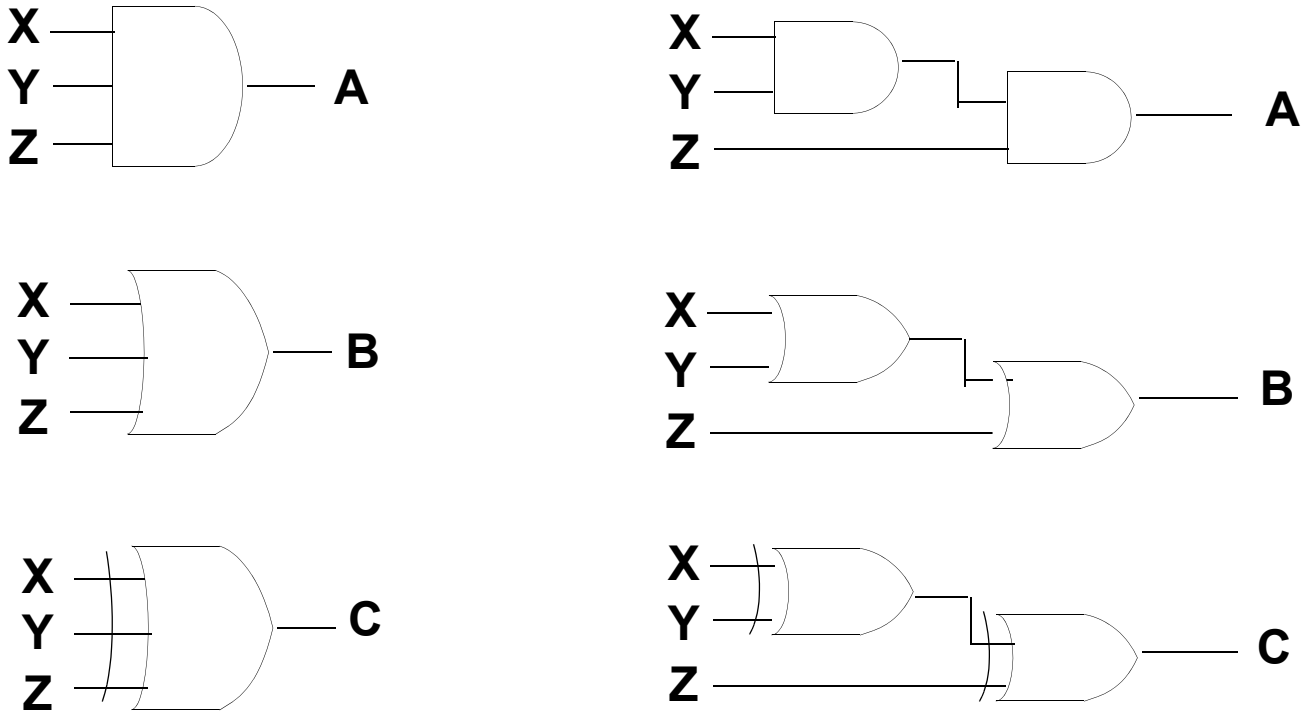
X	Y	Z	W
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1



$W = X \oplus Y \oplus Z$

N-Input Gates

- **N-input gates can be replaced by 2 input gates due to commutative law.**



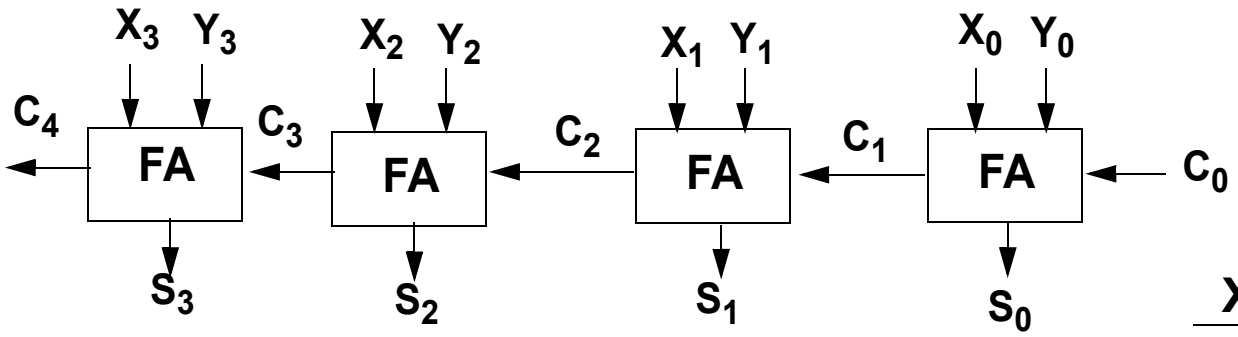
Half Adders Again

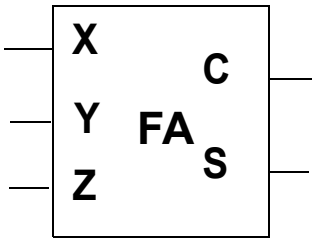
X	Y	C	S
0	**0**	0	**0**
0	**1**	0	**1**
1	**0**	0	**1**
1	**1**	1	**0**

$$S = \overline{X} \cdot Y + X \cdot \overline{Y} = X \oplus Y$$

Full Adders

An half adder plus another input for the carry from the previous lower significant position.

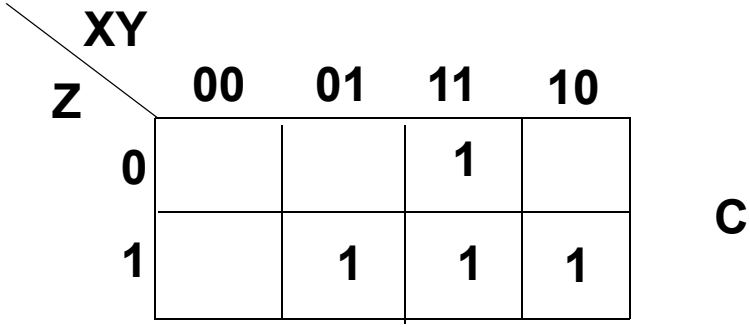


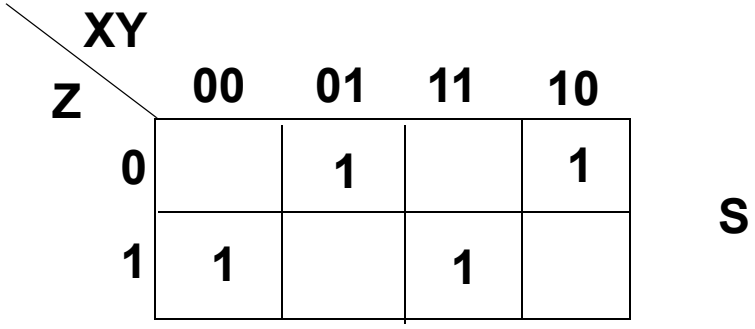


X	Y	Z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

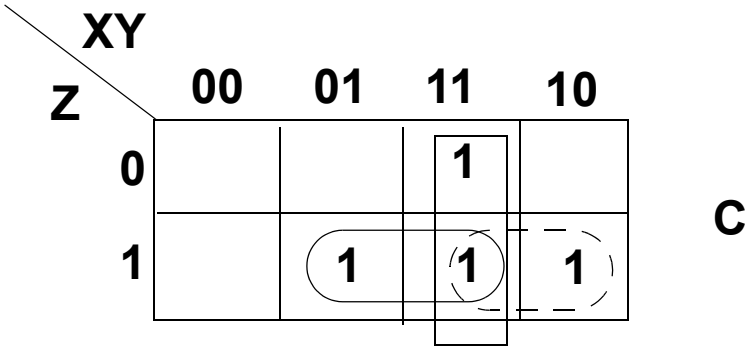
Full Adders Implementation

X	Y	Z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

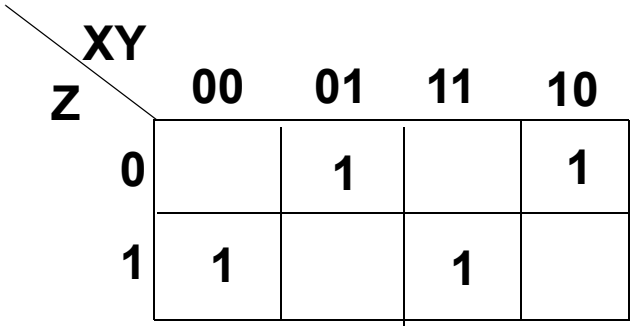




Full Adders Implementation

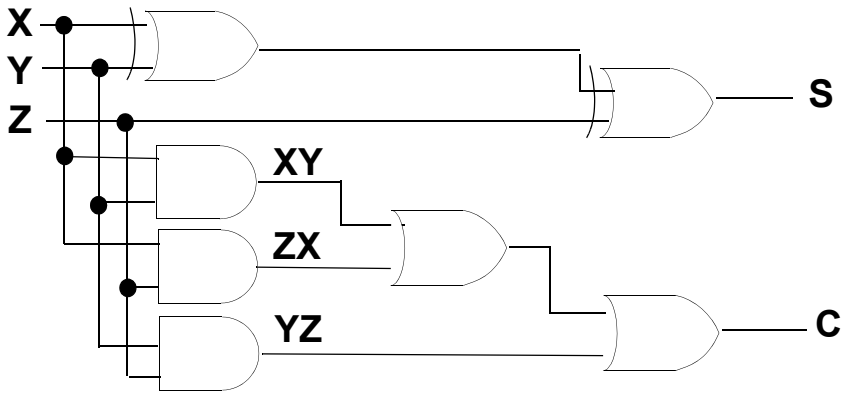


$$C = XY + YZ + XZ$$



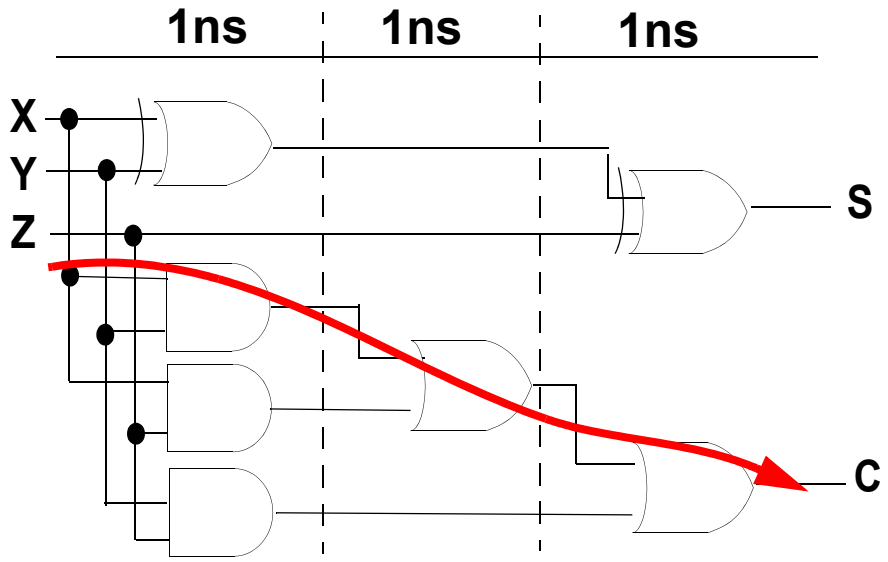
$$S = \overline{X}\cdot\overline{Y}\cdot Z + \overline{X}\cdot Y\cdot\overline{Z} + X\cdot Y\cdot Z + X\cdot\overline{Y}\cdot\overline{Z}$$

$$= X \oplus Y \oplus Z$$



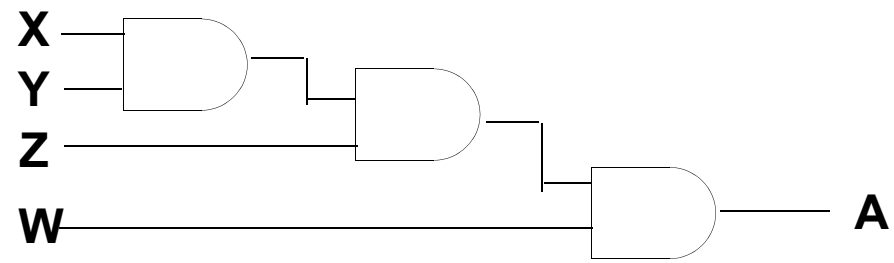
Critical Path of a Combinational Circuit

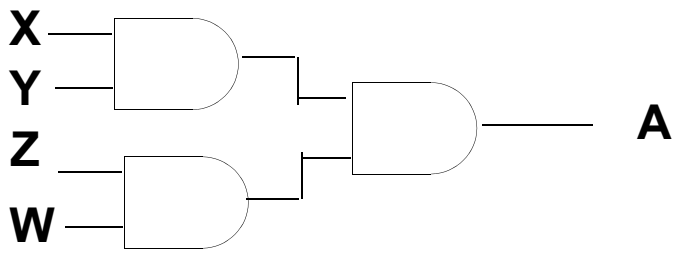
- The time that a circuit takes to generates a result is called the circuit delay.
- If we assume every two input gate takes 1ns, the half adder takes 3ns because it needs to go through 3 gates in worst case.



- A critical path is the path that contains the largest number of gates.

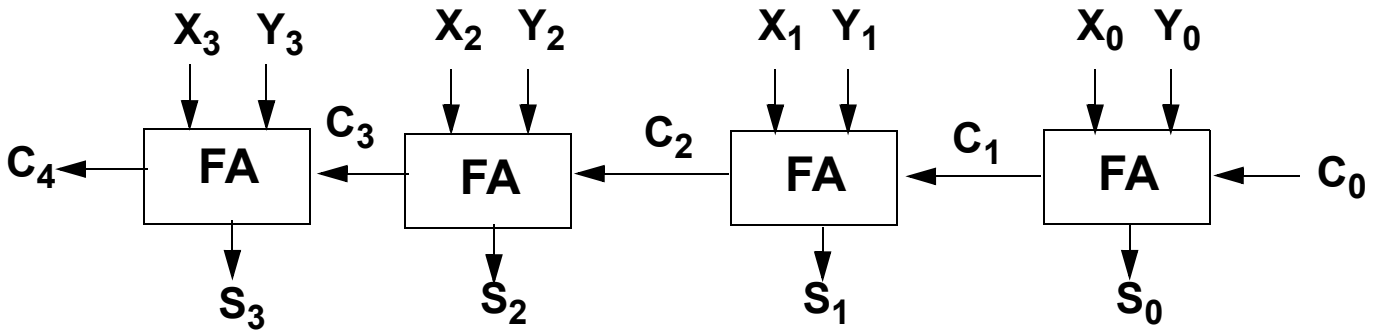
The Circuit with Short Critical Path is Faster.





Ripple Carry Adder (RCA)

- A chain of full adders (FA) is called ripple carry adder (RCA).



- If we assume FA takes 3ns, this RCA takes ? ns to get the final result.

- RCA is slow because each FA needs to wait until it receives a carry value from the previous FA.

Carry Lookahead Adder (CLA)

- **Basic Idea: We can obtain carry values in advance.**
- **Carry c_{i+1} can be generated if one of the following cases occurs.**

  1) x_i and y_i are both 1.

  2) (X_i or Y_i is 1) and C_i is 1.

- **Let's define**

  1) $g_i = x_i y_i$

  2) $p_i = x_i + y_i$

- **Then $c_{i+1} = g_i + p_i c_i$**

$c_1 = g_0 + p_0 c_0$

$c_2 = g_1 + p_1 c_1 = g_1 + p_1 (g_0 + p_0 c_0)$

$c_3 = g_2 + p_2 c_2 = \ldots$

Carry Lookahead Adder (CLA)