Carry Lookahead Adder

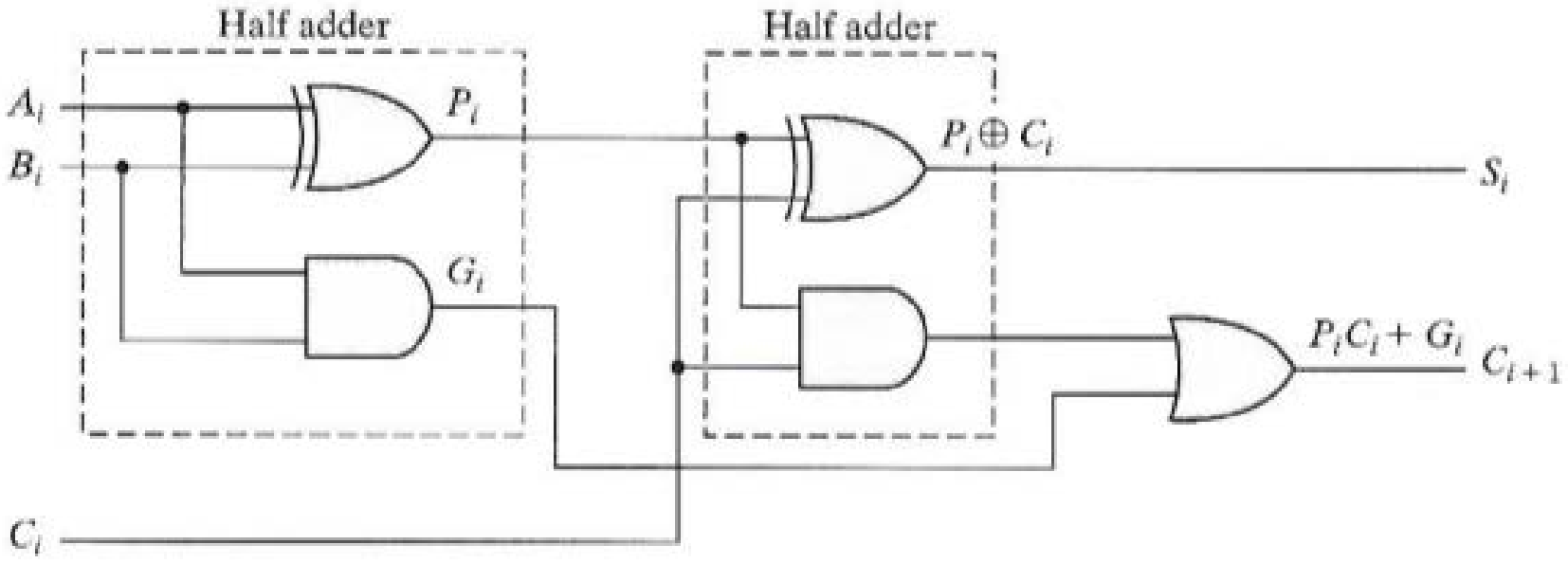
Written by WJ Han

problem

How can you reduce the carry propagation time in a parallel adder.

Design four-bit adder with carry lookahead, the most widely used technique.

Full Adder Inside



Full adder with *P* and *G* shown

carry propagation time

The signal from the input carry C_i to the output carry C_{i+1} propagates through an AND gate and an OR gate, which constitute two gate levels.

The carry propagation time is an important attribute of the adder because it limits the speed with which two numbers are added.

carry lookahead

One solution is to increase the complexity of the equipment in such a way that the carry delay time is reduced.

The most widely used technique employs the principle of carry lookahead logic.

carry output equation

$C_{i+1} = G_i + P_i C_i$

$(P_i = A_i \oplus B_i, \quad G_i = A_i B_i)$

G_i is called a carry generate.

P_i is called a carry propagate, because it determines whether a carry into stage i will propagate into state i+1.

each output carry

$$C_{i+1} = G_i + P_iC_i$$

$$C_1 = G_0 + P_0C_0$$

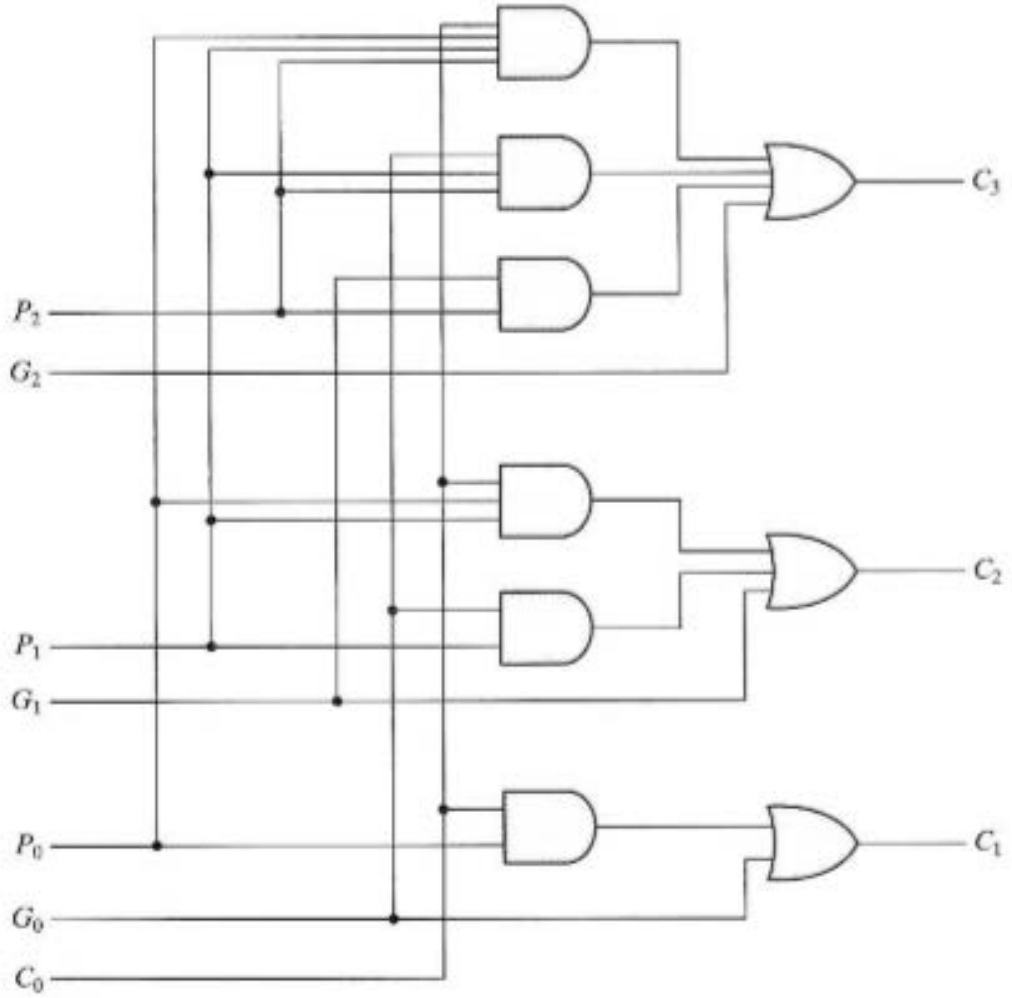
$$C_2 = G_1 + P_1C_1 = P_1(G_0+P_0C_0)$$

$$= G_1 + P_1G_0 + P_1P_0C_0$$

$$C_3 = G_2 + P_2C_2$$

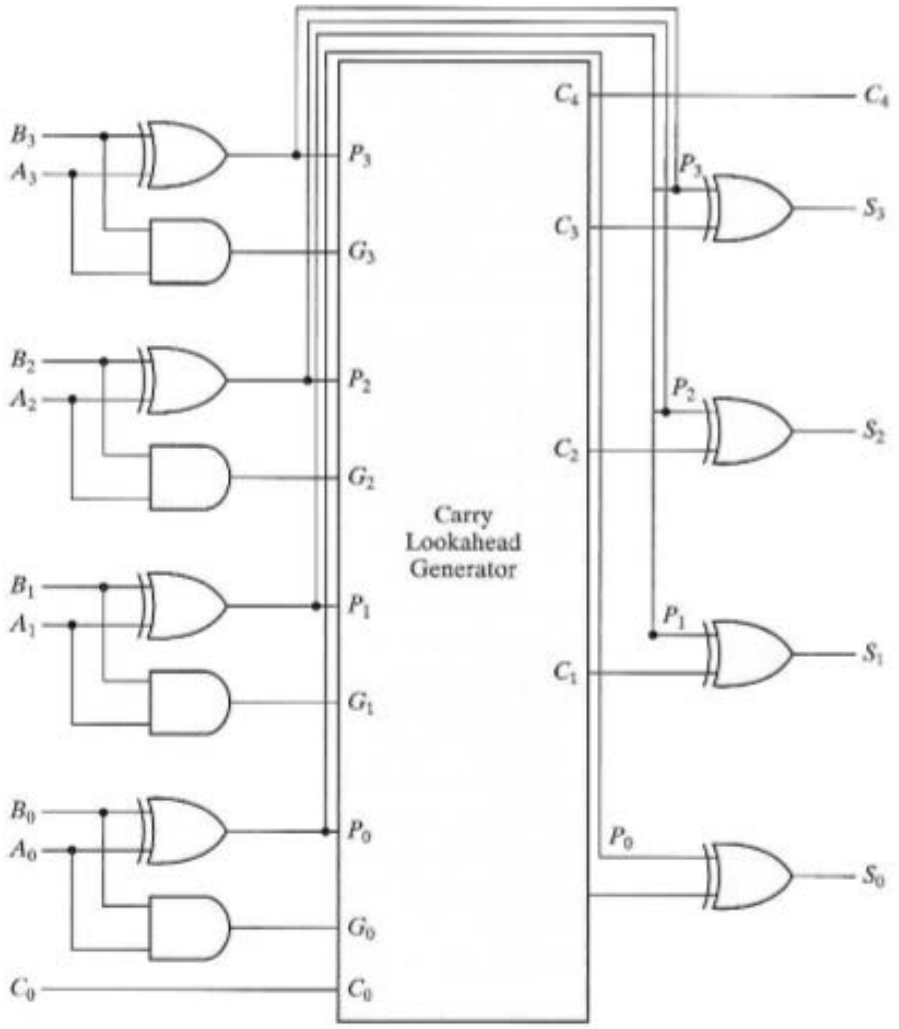
$$= G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_0$$

carry lookahead generator



Logic diagram of carry lookahead generator

4bit adder w. carry lookahead



Four-bit adder with carry lookahead